Proceedings of the 30th IEEE International Symposium on Multiple Valued Logic, Portland, Oregon, USA, 2000, pp.253-258

Evolutionary Multi-Level Network Synthesis in Given Design Style*

T. Łuba

Warsaw University of Technology, POLAND, luba@tele.pw.edu.pl C. Moraga

Dortmund University, GERMANY, moraga@cs.uni-dortmund.de

Yanushkevich

M. Opoka

V. Shmerko

Technical University, Szczecin, POLAND, yanushkevich@wi.ps.pl

Abstract

This mapper extends the technique of evolutionary network design. We study an evolutionary network design strategy from the possition of design style. A hypothesis under investigation is that the uncertainty of a total nearth space (the space of all possible network solutions) through evolutionary network design is removed faster if this space is partitioned into subspaces. This idea has been realized through a parallel window-based scanning of these subspaces. Such a window is determined by the parameters of a multi-level network architecture in a given design style. Our approach allows to conthesize networks with more than two hundred quaternary gates. Moreover, we show that information theoretical interpretation of the evolutionary process is useful, in particular, in partitioning of network space and measuring of fibress function. The experimental data with 6-input quarronary and 11inputs binary benchmarks demonstrate the efficiency of our program, EvoDexign, and an improvement against the recently obtained results.

Introduction

There are different scenarios of network design in Computer Aided Design (CAD) systems, with respect to functions of CAD tools, levels of machine learning support, human-machine interface or, in general, regarding designer's role through the network design process. We solve the problem: generate multi-level logic networks automatically in different design styles. In contrast to recently developed algorithms, we study the proporties that characterize flexibility of network design based on evolutionary paradigm.

The idea of evolutionary network design is very captivating and attractive, because the designer needs no special software to implement a given architecture and design style. These are provided by evolutionary (adaptively) search for the network solution, i.e. the designer becomes an expert. Unfortunately, this idea has been demonstrated on small networks only (2-6 bit multiplexers, 2-5 bit adders and multiplexers, 2-bit decoder, 4-8-state muchine, 3-bit counter) because of many difficulties [1], [6], [9], [11], [12]. A generalization of some aspects toward multiple-valued logic (MVL) networks is known too, for example [7]. More details on current work and trends in evolutionary circuit design can be found in

[&]quot;Supported Impart by visiting grant Philand Belarus Germany from the Committee of Scientific Researches (PDLAND)

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- 1. Understanding the eBook Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - The Rise of Digital Reading Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Advantages of eBooks Over Traditional Books
- 2. Identifying Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
- 3. Choosing the Right eBook Platform

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- User-Friendly Interface
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 - Personalized Recommendations
 - Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings User Reviews and Ratings
 - Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings and Bestseller Lists
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 - Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings Budget-Friendly Options
- 6. Navigating Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logic Proceedings eBook Formats
 - ePub, PDF, MOBI, and More
 - Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings Compatibility with Devices
 - Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Highlighting and Note-Taking Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International

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- Interactive Elements Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
- 8. Staying Engaged with Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
- 9. Balancing eBooks and Physical Books Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium On Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International International Symposium International International
 - Setting Reading Goals Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium On Multiple Valued Logicproceedings
 - Fact-Checking eBook Content of Multiple Valued Logic Ismvl 2000 30th Ieee International Symposium International Symposium On Multiple Valued Logicproceedings
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development

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