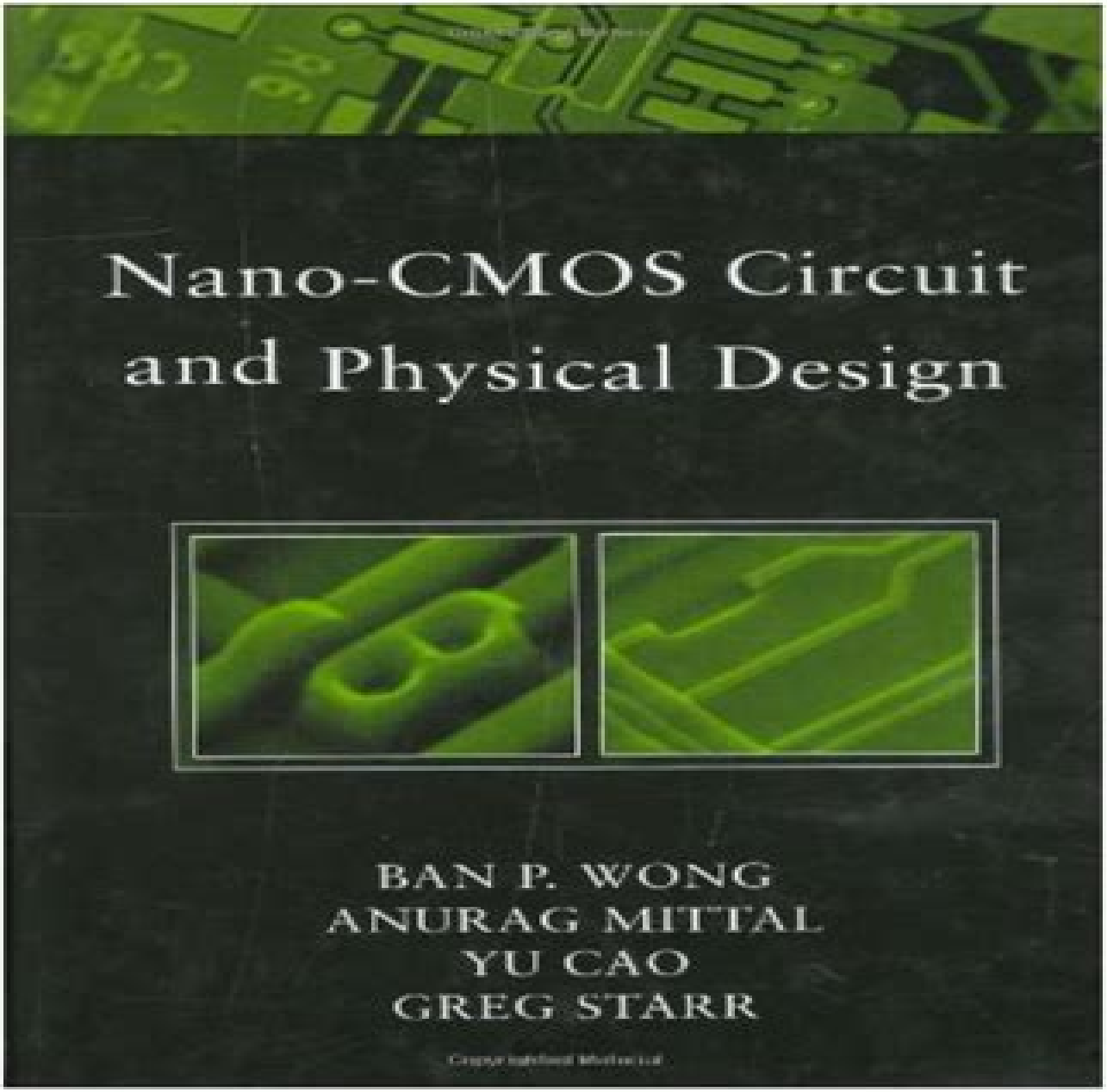
Nano-CMOS Circuit
and Physical Design
BAN P. WONG
ANURAG MITTAL
YU CAO
GREG STARR

Nano Cmos Circuit And Physical Design

Mahtab Niknahad

Nano Cmos Circuit And Physical Design:

Nano-CMOS Circuit and Physical Design Ban Wong,Anurag Mittal,Yu Cao,Greg W. Starr,2005-04-08 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation *Nano-CMOS Design for Manufacturability* Ban P. Wong,Anurag Mittal,Greg W. Starr,Franz Zach,Victor Moroz,Andrew Kahng,2008-12-29 Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano CMOS Design for Manufacturability examines the challenges that design engineers face in the nano scaled era such as exacerbated effects and the proven design for manufacturability DFM methodology in the midst of increasing variability and design process interactions In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore s law the authors also tackle complex issues in the design process to overcome the difficulties including the use of a functional first silicon to support a predictable product ramp Moreover they introduce several emerging concepts including stress proximity effects contour based extraction and design process interactions This book is the sequel to Nano CMOS Circuit and Physical Design taking design to technology nodes beyond 65nm geometries It is divided into three parts Part One Newly Exacerbated Effects introduces the newly exacerbated effects that require designers attention beginning with a discussion of the lithography aspects of DFM followed by the impact of layout on transistor performance Part Two Design Solutions examines how to mitigate the impact of process effects discussing the methodology needed to make sub wavelength patterning technology work in manufacturing as well as design solutions to deal with signal power integrity WELL stress proximity effects and process variability Part Three The Road to DFM describes new tools needed to support DFM efforts including an auto correction tool capable of fixing the layout of cells with multiple optimization goals followed by a look ahead into the future of DFM Throughout the book real world examples simplify complex concepts helping readers see how they can successfully handle projects on Nano CMOS nodes It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and in short make designs that are not only functional but that also meet power and performance goals within the design schedule Nano-CMOS Circuit and Physical Design Ban Wong,2005 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation

Nano-CMOS Design for Manufacturability Ban P. Wong,Anurag Mittal,Greg W. Starr,Franz Zach,Victor Moroz,Andrew

Kahng,2008-10-20 Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano CMOS Design for Manufacturability examines the challenges that design engineers face in the nano scaled era such as exacerbated effects and the proven design for manufacturability DFM methodology in the midst of increasing variability and design process interactions In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore s law the authors also tackle complex issues in the design process to overcome the difficulties including the use of a functional first silicon to support a predictable product ramp Moreover they introduce several emerging concepts including stress proximity effects contour based extraction and design process interactions This book is the sequel to Nano CMOS Circuit and Physical Design taking design to technology nodes beyond 65nm geometries It is divided into three parts Part One Newly Exacerbated Effects introduces the newly exacerbated effects that require designers attention beginning with a discussion of the lithography aspects of DFM followed by the impact of layout on transistor performance Part Two Design Solutions examines how to mitigate the impact of process effects discussing the methodology needed to make sub wavelength patterning technology work in manufacturing as well as design solutions to deal with signal power integrity WELL stress proximity effects and process variability Part Three The Road to DFM describes new tools needed to support DFM efforts including an auto correction tool capable of fixing the layout of cells with multiple optimization goals followed by a look ahead into the future of DFM Throughout the book real world examples simplify complex concepts helping readers see how they can successfully handle projects on Nano CMOS nodes It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and in short make designs that are not only functional but that also meet power and performance goals within the design schedule **Device Circuit Co-Design Issues in FETs** Shubham Tayal,Billel Smaani,Shiromani Balmukund Rahi,Samir Labiod,Zeinab Ramezani,2023-08-22 This book provides an overview of emerging semiconductor devices and their applications in electronic circuits which form the foundation of electronic devices Device Circuit Co Design Issues in FETs provides readers with a better understanding of the ever growing field of low power electronic devices and their applications in the wireless biosensing and circuit domains The book brings researchers and engineers from various disciplines of the VLSI domain together to tackle the emerging challenges in the field of engineering and applications of advanced low power devices in an effort to improve the performance of these technologies The chapters examine the challenges and scope of FinFET device circuits 3D FETs and advanced FET for circuit applications The book also discusses low power memory design neuromorphic computing and issues related to thermal reliability The authors provide a good understanding of device physics and circuits and discuss transistors based on the new channel dielectric materials and device architectures to achieve low power dissipation and ultra high switching speeds to fulfill the requirements of the semiconductor industry This book is intended for students researchers and professionals in the field of semiconductor devices and nanodevices as well as those working on device circuit co design

issues **Circuits at the Nanoscale** Krzysztof Iniewski,2018-10-08 Circuits for Emerging Technologies Beyond CMOS New exciting opportunities are abounding in the field of body area networks wireless communications data networking and optical imaging In response to these developments top notch international experts in industry and academia present Circuits at the Nanoscale Communications Imaging and Sensing This volume unique in both its scope and its focus addresses the state of the art in integrated circuit design in the context of emerging systems A must for anyone serious about circuit design for future technologies this book discusses emerging materials that can take system performance beyond standard CMOS These include Silicon on Insulator SOI Silicon Germanium SiGe and Indium Phosphide InP Three dimensional CMOS integration and co integration with Microelectromechanical MEMS technology and radiation sensors are described as well Topics in the book are divided into comprehensive sections on emerging design techniques mixed signal CMOS circuits circuits for communications and circuits for imaging and sensing Dr Krzysztof Iniewski is a director at CMOS Emerging Technologies Inc a consulting company in Vancouver British Columbia His current research interests are in VLSI ciruits for medical applications He has published over 100 research papers in international journals and conferences and he holds 18 international patents granted in the United States Canada France Germany and Japan In this volume he has assembled the contributions of over 60 world reknown experts who are at the top of their field in the world of circuit design advancing the bank of knowledge for all who work in this exciting and burgeoning area **Process Variations and Probabilistic Integrated Circuit Design** Manfred Dietrich,Joachim Haase,2011-11-20 Uncertainty in key parameters within a chip and between different chips in the deep sub micron area plays a more and more important role As a result manufacturing process spreads need to be considered during the design process Quantitative methodology is needed to ensure faultless functionality despite existing process variations within given bounds during product development This book presents the technological physical and mathematical fundamentals for a design paradigm shift from a deterministic process to a probability orientated design process for microelectronic circuits Readers will learn to evaluate the different sources of variations in the design flow in order to establish different design variants while applying appropriate methods and tools to evaluate and optimize their design Flip-Flop Design in Nanometer CMOS Massimo Alioto,Elio Consoli,Gaetano Palumbo,2014-10-14 This book provides a unified treatment of Flip Flop design and selection in nanometer CMOS VLSI systems The design aspects related to the energy delay tradeoff in Flip Flops are discussed including their energy optimal selection according to the targeted application and the detailed circuit design in nanometer CMOS VLSI systems Design strategies are derived in a coherent framework that includes explicitly nanometer effects including leakage layout parasitics and process voltage temperature variations as main advances over the existing body of work in the field The related design tradeoffs are explored in a wide range of applications and the related energy performance targets A wide range of existing and recently proposed Flip Flop topologies are discussed Theoretical foundations are provided to set the stage for the derivation of design guidelines and

emphasis is given on practical aspects and consequences of the presented results Analytical models and derivations are introduced when needed to gain an insight into the inter dependence of design parameters under practical constraints This book serves as a valuable reference for practicing engineers working in the VLSI design area and as text book for senior undergraduate graduate and postgraduate students already familiar with digital circuits and timing **High-k Gate Dielectrics for CMOS Technology** Gang He,Zhaoqi Sun,2012-08-10 A state of the art overview of high k dielectric materials for advanced field effect transistors from both a fundamental and a technological viewpoint summarizing the latest research results and development solutions As such the book clearly discusses the advantages of these materials over conventional materials and also addresses the issues that accompany their integration into existing production technologies Aimed at academia and industry alike this monograph combines introductory parts for newcomers to the field as well as advanced sections with directly applicable solutions for experienced researchers and developers in materials science physics and electrical engineering Computational and Ambient Intelligence Francisco Sandoval,Alberto Prieto,Joan Cabestany,Manuel Graña,2007-09-21 This book constitutes the refereed proceedings of the 9th International Work Conference on Artificial Neural Networks IWANN 2007 held in San Sebasti n Spain in June 2007 Coverage includes theoretical concepts and neurocomputational formulations evolutionary and genetic algorithms data analysis signal processing robotics and planning motor control as well as neural networks and other machine learning methods in cancer research Handbook of 3D Integration, Volume 1 Philip Garrou,Christopher Bower,Peter Ramm,2011-09-22 The first encompassing treatise of this new but very important field puts the known physical limitations for classic 2D electronics into perspective with the requirements for further electronics developments and market necessities This two volume handbook presents 3D solutions to the feature density problem addressing all important issues such as wafer processing die bonding packaging technology and thermal aspects It begins with an introductory part which defines necessary goals existing issues and relates 3D integration to the semiconductor roadmap of the industry Before going on to cover processing technology and 3D structure fabrication strategies in detail This is followed by fields of application and a look at the future of 3D integration The contributions come from key players in the field from both academia and industry including such companies as Lincoln Labs Fraunhofer RPI ASET IMEC CEA LETI IBM and Renesas *Semiconductor Devices and Technologies for Future Ultra Low Power Electronics* D. Nirmal,J. Ajayan,Patrick J. Fay,2021-12-09 This book covers the fundamentals and significance of 2 D materials and related semiconductor transistor technologies for the next generation ultra low power applications It provides comprehensive coverage on advanced low power transistors such as NCFETs FinFETs TFETs and flexible transistors for future ultra low power applications owing to their better subthreshold swing and scalability In addition the text examines the use of field effect transistors for biosensing applications and covers design considerations and compact modeling of advanced low power transistors such as NCFETs FinFETs and TFETs TCAD simulation examples are also

provided FEATURES Discusses the latest updates in the field of ultra low power semiconductor transistors Provides both experimental and analytical solutions for TFETs and NCFETs Presents synthesis and fabrication processes for FinFETs Reviews details on 2 D materials and 2 D transistors Explores the application of FETs for biosensing in the healthcare field This book is aimed at researchers professionals and graduate students in electrical engineering electronics and communication engineering electron devices nanoelectronics and nanotechnology microelectronics and solid state circuits

Design Rules in a Semiconductor Foundry Eitan N. Shauly,2022-11-30 Nowadays over 50% of integrated circuits are fabricated at wafer foundries This book presents a foundry integrated perspective of the field and is a comprehensive and up to date manual designed to serve process device layout and design engineers It comprises chapters carefully selected to cover topics relevant for them to deal with their work The book provides an insight into the different types of design rules DRs and considerations for setting new DRs It discusses isolation gate patterning S D contacts metal lines MOL air gaps and so on It explains in detail the layout rules needed to support advanced planarization processes different types of dummies and related utilities as well as presents a large set of guidelines and layout aware modeling for RF CMOS and analog modules It also discusses the layout DRs for different mobility enhancement techniques and their related modeling listing many of the dedicated rules for static random access memory SRAM embedded polyfuse ePF and LogicNVM The book also provides the setting and calibration of the process parameters set and describes the 28 20 nm planar MOSFET process flow for low power and high performance mobile applications in a step by step manner It includes FEOL and BEOL physical and environmental tests for qualifications together with automotive qualification and design for automotive DfA Written for the professionals the book belongs to the bookshelf of microelectronic discipline experts *Digitally-Assisted Analog and Analog-Assisted Digital IC Design* Xicheng Jiang,2015-07-23 Achieve enhanced performance with this guide to cutting edge techniques for digitally assisted analog and analog assisted digital integrated circuit design Discover how architecture and circuit innovations can deliver improved performance in terms of speed density power and cost Learn about practical design considerations for high performance scaled CMOS processes FinFet devices and architectures and the implications of FD SOI technology Get up to speed with established circuit techniques that take advantage of scaled CMOS process technology in analog digital RF and SoC designs including digitally assisted techniques for data converters DSP enabled frequency synthesizers and digital controllers for switching power converters With detailed descriptions explanations and practical advice from leading industry experts this is an ideal resource for practicing engineers researchers and graduate students working in circuit design **Low-Power High-Level Synthesis for Nanoscale CMOS Circuits** Saraju P. Mohanty,Nagarajan Ranganathan,Elias Kougianos,Priyardarsan Patra,2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale

integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits

Using Fine Grain Approaches for Highly Reliable Design of FPGA-based Systems in Space Mahtab Niknahad,2014-05-22 Nowadays using SRAM based FPGAs in space missions is increasingly considered due to their flexibility and reprogrammability A challenge is the devices sensitivity to radiation effects that increased with modern architectures due to smaller CMOS structures This work proposes fault tolerance methodologies that are based on a fine grain view to modern reconfigurable architectures The focus is on SEU mitigation challenges in SRAM based FPGAs which can result in crucial situations *System-on-Chip Test Architectures* Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots

Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students **Timing Performance of Nanometer Digital Circuits Under Process Variations** Victor Champac,Jose Garcia Gervacio,2018-04-18 This book discusses the digital design of integrated circuits under process variations with a focus on design time solutions The authors describe a step by step methodology going from logic gates to logic paths to the circuit level Topics are presented in comprehensively without overwhelming use of analytical formulations Emphasis is placed on providing digital designers with understanding of the sources of process variations their impact on circuit performance and tools for improving their designs to comply with product specifications Various circuit level design hints are highlighted so that readers can use then to improve their designs A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits This book enables readers to make optimal decisions at design time toward more efficient circuits with better yield and higher reliability **Design for Manufacturability** Artur Balasinski,2013-10-05 This book explains integrated circuit design for manufacturability DfM at the product level packaging applications and applies engineering DfM principles to the latest standards of product development at 22 nm technology nodes It is a valuable guide for layout designers packaging engineers and quality engineers covering DfM development from 1D to 4D involving IC design flow setup best practices links to manufacturing and product definition for process technologies down to 22 nm node and product families including memories logic system on chip and system in package Low-Dimensional Nanoelectronic Devices Angsuman Sarkar,Arpan Deyasi,2022-10-27 Providing cutting edge research on nanoelectronics and photonic devices and its application in future integrated circuits this state of the art book tackles the challenges of the different detailed theoretical and analytical models of solving the problems of various nanodevices The volume also explores from different angles the roles of material composition and choice of materials that now play the most critical role in determining outcomes of low dimensional nanoelectronic devices The applications of those findings are extremely beneficial for the computing and telecommunication industries Beginning with a solid theoretical background for every chapter this volume covers the hottest areas of present day electronic engineering The continuous miniaturization of devices components and systems requires corresponding cutting edge theoretical analysis supported by simulated findings before actual fabrication That purpose is given maximum focus in this volume which has interdisciplinary appeal making it a comprehensive technological volume that deals with underlying aspects of physics materials structures in nano regime and the corresponding end product in the form of devices

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