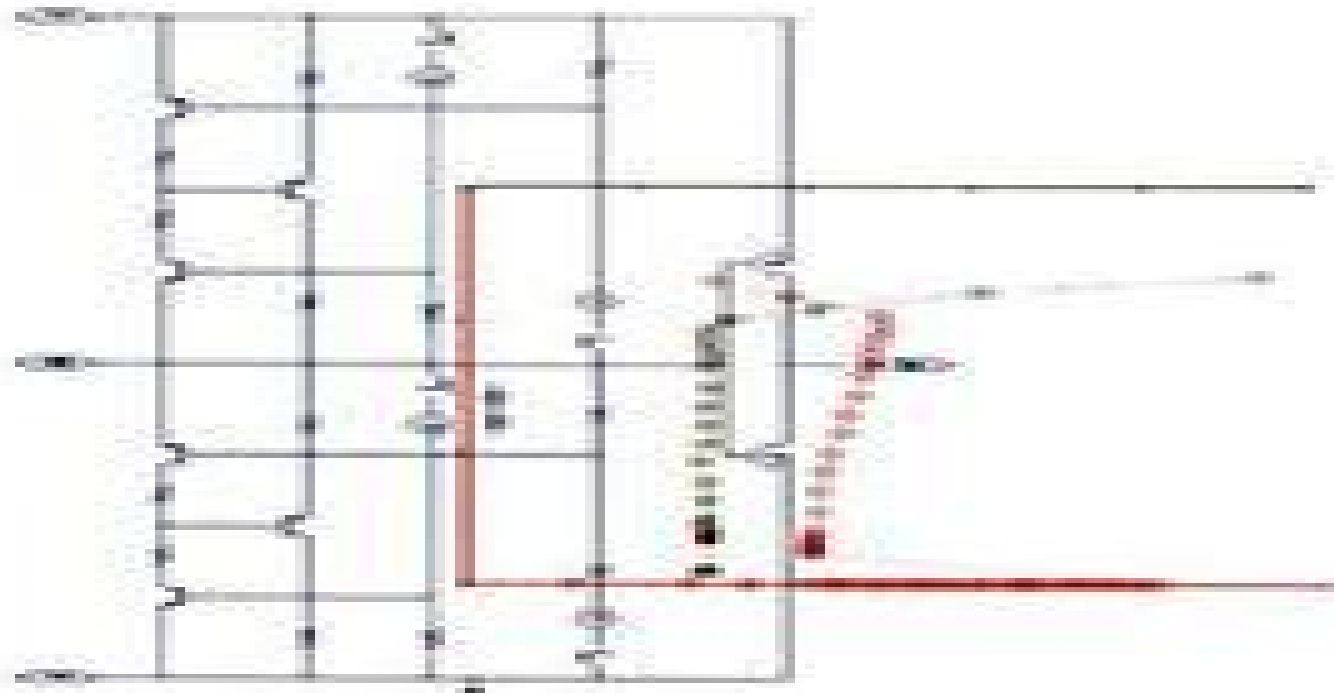


ON-CHIP ESD PROTECTION FOR INTEGRATED CIRCUITS

An IC Design Perspective



Albert Z. H. Wang

On Chip ESD Protection For Integrated Circuits An Ic Design Perspective

**Amit Patra, Shailendra Baranwal, Ashis
Maity, Samiran Dam, Syed Asif Eqbal**

On Chip ESD Protection For Integrated Circuits An Ic Design Perspective:

On-Chip ESD Protection for Integrated Circuits Albert Z.H. Wang, 2006-01-03 This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer's perspective. On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits including Testing models and standards adopted by U.S. Department of Defense EIA JEDEC ESD Association Automotive Electronics Council International Electrotechnical Commission etc. ESD failure analysis protection devices and protection of sub-circuits. Whole chip ESD protection and ESD to circuit interactions. Advanced low parasitic compact ESD protection structures for RF and mixed signal IC's. Mixed mode ESD simulation design methodologies for design prediction. ESD to circuit interactions and more. Many real world ESD protection circuit design examples are provided. The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field.

On-Chip ESD Protection for Integrated Circuits Albert Z.H. Wang, 2002-01-31 This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer's perspective. On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits including Testing models and standards adopted by U.S. Department of Defense EIA JEDEC ESD Association Automotive Electronics Council International Electrotechnical Commission etc. ESD failure analysis protection devices and protection of sub-circuits. Whole chip ESD protection and ESD to circuit interactions. Advanced low parasitic compact ESD protection structures for RF and mixed signal IC's. Mixed mode ESD simulation design methodologies for design prediction. ESD to circuit interactions and more. Many real world ESD protection circuit design examples are provided. The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field.

On-Chip ESD Protection for Integrated Circuits Albert Z. H. Wang, 2014-01-15 Practical ESD Protection Design Albert Wang, 2022-01-06 An authoritative single volume reference on the design and analysis of ESD protection for ICs. Electrostatic discharge (ESD) is a major reliability challenge to semiconductors, integrated circuits (ICs) and microelectronic systems. On-chip ESD protection is a vital to any electronic products such as smartphones, laptops, tablets and other electronic devices. Practical ESD Protection Design provides comprehensive and systematic guidance on all major aspects of designs of on-chip ESD protection for integrated circuits (ICs). Written for students and practicing engineers alike, this one-stop resource covers essential theories, hands-on design skills, computer-aided design (CAD) methods, characterization and analysis techniques and more on ESD protection designs. Detailed chapters examine an array of topics ranging from fundamental to advanced, including ESD phenomena, ESD failure analysis, ESD testing models, ESD protection devices and circuits, ESD design layout and technology effects, ESD design flows and co-design methods, ESD modelling and CAD techniques and future ESD protection concepts. Based on the author's decades of design research and teaching experiences.

Practical ESD Protection Design Features numerous real world ESD protection design examples Emphasizes on ESD protection design techniques and procedures Describes ESD IC co design methodology for high performance mixed signal ICs and broadband radio frequency RF ICs Discusses CAD based ESD protection design optimization and prediction using both Technology and Electrical Computer Aided Design TCAD ECAD simulation Addresses new ESD CAD algorithms and tools for full chip ESD physical design verification Explores the disruptive future outlook of ESD protection Practical ESD Protection Design is a valuable reference for industrial engineers and academic researchers in the field and an excellent textbook for electronic engineering courses in semiconductor microelectronics and integrated circuit designs

Analog Circuit Design Arthur H.M. van Roermund, Michiel Steyaert, Johan Huijsing, 2005-12-30 Number 12 in the successful series of Analog Circuit Design provides valuable information and excellent overviews of analogue circuit design CAD and RF systems The series is an ideal reference for those involved in analogue and mixed signal design

Parasitic Substrate Coupling in High Voltage Integrated Circuits Pietro Buccella, Camillo Stefanucci, Maher Kayal, Jean-Michel Sallese, 2018-03-14 This book introduces a new approach to model and predict substrate parasitic failures in integrated circuits with standard circuit design tools The injection of majority and minority carriers in the substrate is a recurring problem in smart power ICs containing high voltage high current switching devices besides sensitive control protection and signal processing circuits The injection of parasitic charges leads to the activation of substrate bipolar transistors This book explores how these events can be evaluated for a wide range of circuit topologies To this purpose new generalized devices implemented in Verilog A are used to model the substrate with standard circuit simulators This approach was able to predict for the first time the activation of a latch up in real circuits through post layout SPICE simulation analysis Discusses substrate modeling and circuit level simulation of parasitic bipolar device coupling effects in integrated circuits Includes circuit back annotation of the parasitic lateral n p n and vertical p n p bipolar transistors in the substrate Uses Spice for simulation and characterization of parasitic bipolar transistors latch up of the parasitic p n p n structure and electrostatic discharge ESD protection devices Offers design guidelines to reduce couplings by adding specific protections

Microfabricated Systems and MEMS VII, 2004 **Handbook of Automotive Power Electronics and Motor Drives** Ali Emadi, 2017-12-19 Initially the only electric loads encountered in an automobile were for lighting and the starter motor Today demands on performance safety emissions comfort convenience entertainment and communications have seen the working in of seemingly innumerable advanced electronic devices Consequently vehicle electric systems require larger capacities and more complex configurations to deal with these demands Covering applications in conventional hybrid electric and electric vehicles the Handbook of Automotive Power Electronics and Motor Drives provides a comprehensive reference for automotive electrical systems This authoritative handbook features contributions from an outstanding international panel of experts from industry and academia highlighting existing and emerging technologies Divided into five parts the Handbook

of Automotive Power Electronics and Motor Drives offers an overview of automotive power systems discusses semiconductor devices sensors and other components explains different power electronic converters examines electric machines and associated drives and details various advanced electrical loads as well as battery technology for automobile applications As we seek to answer the call for safer more efficient and lower emission vehicles from regulators and consumer insistence on better performance comfort and entertainment the technologies outlined in this book are vital for engineering advanced vehicles that will satisfy these criteria

Electromagnetic Compatibility of Integrated Circuits Sonia Ben Dhia, Mohamed Ramdani, Etienne Sicard, 2006-06-04 Electromagnetic Compatibility of Integrated Circuits Techniques for Low Emission and Susceptibility focuses on the electromagnetic compatibility of integrated circuits The basic concepts theory and an extensive historical review of integrated circuit emission and susceptibility are provided Standardized measurement methods are detailed through various case studies EMC models for the core I/Os supply network and packaging are described with applications to conducted switching noise signal integrity near field and radiated noise Case studies from different companies and research laboratories are presented with in depth descriptions of the ICs test set ups and comparisons between measurements and simulations Specific guidelines for achieving low emission and susceptibility derived from the experience of EMC experts are presented

Contamination and ESD Control in High-Technology Manufacturing Roger W. Welker, R. Nagarajan, Carl E. Newberg, 2006-09-18 A practical how to guide that effectively deals with the control of both contamination and ESD This book offers effective strategies and techniques for contamination and electrostatic discharge ESD control that can be implemented in a wide range of high technology industries including semiconductor disk drive aerospace pharmaceutical medical device automobile and food production manufacturing The authors set forth a new and innovative methodology that can manage both contamination and ESD often considered to be mutually exclusive challenges requiring distinct strategies Beginning with two general chapters on the fundamentals of contamination and ESD control the book presents a logical progression of topics that collectively build the necessary skills and knowledge Analysis methods for solving contamination and ESD problems Building the contamination and ESD control environment including design and construction of cleanrooms and ESD protected environments Cleaning processes and the equipment needed to support these processes Tooling design and certification Continuous monitoring Consumable supplies and packaging materials Controlling contamination and ESD originating from people Management of cleanrooms and ESD protected workplace environments Contamination and ESD Control in High Technology Manufacturing conveys a practical working knowledge of contamination and ESD control strategies and techniques and it is filled with case studies that illustrate key principles and the benefits of contamination and ESD control Moreover its straightforward style makes the material which integrates many disciplines of engineering and science clear and accessible Written by three leading industry experts this book is an essential guide for engineers and designers across the many industries where contamination and ESD

control is a concern *IEICE Transactions on Electronics*, 2002

Proceedings of the ... International Symposium on ESD Design Challenges and Strategies in

Deeply-scaled Integrated Circuits Shuqing Cao, 2010 It is the main objective of this work to address the scaling and design challenges of ESD protection in deeply scaled technologies First the thesis introduces the on chip ESD events the scaling and design challenges and the nomenclatures necessary for later chapters The ESD design window and the I/O schematics for both rail clamping and local clamping ESD schemes are illustrated Then the thesis delves into the investigation of the input and output driver devices and examines their robustness under ESD The input driver's oxide breakdown levels are evaluated in deeply scaled technologies The output driver's trigger and breakdown voltages are improved appreciably by applying circuit and device design techniques The ESD device sections first discuss rail based clamping a widely used protection scheme Two diode based devices namely the gated diode and substrate diode are investigated in detail with SOI test structures Characterization is based on DC current voltage I-V Very Fast Transmission Line Pulse VF-TLP capacitance and leakage measurements Improvements in performance are realized Technology computer aided design TCAD simulations help understand the physical effects and design tradeoffs Then the following section focuses on the local clamping scheme Two devices the field effect diode FED and the double well FED DWFED are developed and optimized in an SOI technology Trigger circuits are designed to improve the turn on speed The advantages of local clamping is highlighted and compared with the rail based clamping The results show that the FED is a suitable option for power clamping applications and the DWFED is most suitable for pad based local clamping The thesis presents an ESD protection design methodology which takes advantage of the results and techniques from previous chapters and put each element into a useful format Based on the correlation of package level and in lab test results a design process based on CDM target definition and device optimization discharge path analysis parasitic minimization I/O data rate estimation and finally ESD and performance characterization is used sequentially to systematically realize the overall design goals **Practical ESD**

Protection Design Albert Wang, 2021-12-07 An authoritative single volume reference on the design and analysis of ESD protection for ICs Electrostatic discharge ESD is a major reliability challenge to semiconductors integrated circuits ICs and microelectronic systems On chip ESD protection is a vital to any electronic products such as smartphones laptops tablets and other electronic devices Practical ESD Protection Design provides comprehensive and systematic guidance on all major aspects of designs of on chip ESD protection for integrated circuits ICs Written for students and practicing engineers alike this one stop resource covers essential theories hands on design skills computer aided design CAD methods characterization and analysis techniques and more on ESD protection designs Detailed chapters examine an array of topics ranging from fundamental to advanced including ESD phenomena ESD failure analysis ESD testing models ESD protection devices and circuits ESD design layout and technology effects ESD design flows and co design methods ESD modelling and CAD

techniques and future ESD protection concepts Based on the author s decades of design research and teaching experiences Practical ESD Protection Design Features numerous real world ESD protection design examples Emphasizes on ESD protection design techniques and procedures Describes ESD IC co design methodology for high performance mixed signal ICs and broadband radio frequency RF ICs Discusses CAD based ESD protection design optimization and prediction using both Technology and Electrical Computer Aided Design TCAD ECAD simulation Addresses new ESD CAD algorithms and tools for full chip ESD physical design verification Explores the disruptive future outlook of ESD protection Practical ESD Protection Design is a valuable reference for industrial engineers and academic researchers in the field and an excellent textbook for electronic engineering courses in semiconductor microelectronics and integrated circuit designs

Proceedings ,2005 **The British National Bibliography** Arthur James Wells,2003 **System Level ESD**

Protection Vladislav Vashchenko,Mirko Scholz,2014-03-21 This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge ESD protection It is an invaluable reference for anyone developing systems on chip SoC and systems on package SoP integrated with system level ESD protection The book focuses on both the design of semiconductor integrated circuit IC components with embedded on chip system level protection and IC system co design The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits thereby reducing or completely eliminating the need for additional discrete components on the printed circuit board PCB and meeting system level ESD requirements The authors take a systematic approach based on IC system ESD protection co design A detailed description of the available IC level ESD testing methods is provided together with a discussion of the correlation between IC level and system level ESD testing methods The IC level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing The overall methodology for IC system ESD co design is presented as a step by step procedure that involves both ESD testing and numerical simulations

System Level ESD Co-Design Charvaka Duvvury,Harald Gossner,2017-05-05 An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000 4 2 is paramount for any system design This pioneering book presents the collective knowledge of system designers and system testing experts and state of the art techniques for achieving efficient system level ESD protection with minimum impact on the system performance All categories of system failures ranging from hard to soft types are considered to review simulation and tool applications that can be used The principal focus of System Level ESD Co Design is defining and establishing the importance of co design efforts from both IC supplier and system builder perspectives ESD designers often face challenges in meeting customers system level ESD requirements and therefore a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance With contributions from Robert Ashton Jeffrey Dunnihoo Micheal Hopkins Pratik Maheshwari David Pomerence Wolfgang Reinprecht and Matti Usumaki

readers benefit from hands on experience and in depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD robust systems that include mobile and automotive applications The first dedicated resource to system level ESD co design this is an essential reference for industry ESD designers system builders IC suppliers and customers and also Original Equipment Manufacturers OEMs Key features Clarifies the concept of system level ESD protection Introduces a co design approach for ESD robust systems Details soft and hard ESD fail mechanisms Detailed protection strategies for both mobile and automotive applications Explains simulation tools and methodology for system level ESD co design and overviews available test methods and standards Highlights economic benefits of system ESD co design

Power Management Integrated Circuits Amit Patra, Shailendra Baranwal, Ashis Maity, Samiran Dam, Syed Asif Eqbal, 2024-09-09 This book intends to be a comprehensive text on the topic of integrated circuits for power management putting together both theoretical foundations and practical details leading to successful design practices in research and industry It covers all the three main categories of power management circuits viz linear regulators inductor based switchers and switched capacitor circuits and presents detailed discussion of their common topologies operation and modeling Features Includes underlying theory and design implementation practical ingredients for power management integrated circuits PMICs Provides in depth analysis of topologies and circuits related to linear regulators switched capacitor converters and inductor based converters Covers all the relevant topics at the intersection between power electronics and integrated circuit design areas Provides guidelines for design of circuits and solutions for all the pertinent topologies Indicates all important issues and the related trade offs in the design of PMICs The book will be a valuable resource for senior and graduate level students as well as industry professionals who have done university level courses on analog circuit design control systems and power electronics

ESD in Silicon Integrated Circuits E. Ajith Amerasekera, Charvaka Duvvury, 1995 ESD in Silicon Integrated Circuits Ajith Amerasekera Charvaka Duvvury Texas Instruments Inc Dallas USA Electrostatic Discharge ESD effects in silicon integrated circuits have become a major concern as today's high circuit density technologies shrink to sub micro dimensions This book provides an understanding of the basic features related to ESD and deals with topics ranging from the physics of devices operating under ESD conditions to approaches for solving and improving ESD performance in advanced ICs Features include Description of the methods used to reproduce ESD type events in a controlled test environment Analysis of the behavior of different semiconductor devices under ESD conditions including the physics and modeling of devices Detailed study of design and layout requirements for ESD protection circuits Case studies showing examples of approaches to solving ESD design problems including failure analysis Covering the state of the art in circuit design for ESD prevention this practical book is written from an industrial perspective and will appeal to engineers and scientists working in the fields of IC and transistor design Researchers and advanced students in the fields of device circuit modeling and semiconductor reliability seeking to

understand the fundamentals of ESD phenomena will also find this book an invaluable reference source

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