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GIOVANNI DE MICHELI LUCA BENINI



Networks On Chips Technology And Tools Systems On Silicon

David Wolpert, Paul Ampadu



Networks On Chips Technology And Tools Systems On Silicon:

Networks on Chips Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today's semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems. These highly complex systems on chips demand new approaches to connect and manage the communication between on-chip processing and storage components and networks on chips. NoCs provide a powerful solution. This book is the first to provide a unified overview of NoC technology. It includes in-depth analysis of all the on-chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and solutions. Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends. An integrated presentation not currently available in any other book. A thorough introduction to current design methodologies and chips designed with NoCs. [Designing Network On-Chip Architectures in the Nanoscale Era](#) Jose Flich, Davide Bertozzi, 2010-12-18 Going beyond isolated research ideas and design experiences. *Designing Network On Chip Architectures in the Nanoscale Era* covers the foundations and design methods of network on chip NoC technology. The contributors draw on their own lessons learned to provide strong practical guidance on various design issues. Exploring the design process of the **Debugging Systems-on-Chip** Bart Vermeulen, Kees Goossens, 2014-07-14 This book describes an approach and supporting infrastructure to facilitate debugging the silicon implementation of a System on Chip SOC allowing its associated product to be introduced into the market more quickly. Readers learn step by step the key requirements for debugging a modern silicon SOC implementation: nine factors that complicate this debugging task and a new debug approach that addresses these requirements and complicating factors. The authors' novel communication-centric scan-based abstraction-based run-stop-based CSAR debug approach is discussed in detail showing how it helps to meet debug requirements and address the nine previously identified factors that complicate debugging silicon implementations of SOC's. The authors also derive the debug infrastructure requirements to support debugging of a silicon implementation of an SOC with their CSAR debug approach. This debug infrastructure consists of a generic on-chip debug architecture, a configurable automated design for debug flow to be used during the design of an SOC and customizable off-chip debugger software. Coverage includes an evaluation of the efficiency and effectiveness of the CSAR approach and its supporting infrastructure using six industrial SOC's and an illustrative example SOC model. The authors also quantify the hardware cost and design effort to support their approach. **Reliability, Availability and Serviceability of Networks-on-Chip** Érika Cota, Alexandre de Moraes Amory, Marcelo Soares Lubaszewski, 2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems. It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems, challenges, solutions and trade-offs related to designing and implementing state of the art on-chip communication architectures. **Designing 2D and 3D**

Network-on-Chip Architectures Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies

Encyclopedia of Information Science and Technology, Third Edition Khosrow-Pour, D.B.A., Mehdi,2014-07-31 This 10 volume compilation of authoritative research based articles contributed by thousands of researchers and experts from all over the world emphasized modern issues and the presentation of potential opportunities prospective solutions and future directions in the field of information science and technology Provided by publisher

Modeling, Analysis and Optimization of Network-on-Chip Communication Architectures Umit Y. Ogras,Radu Marculescu,2013-03-12 Traditionally design space exploration for Systems on Chip SoCs has focused on the computational aspects of the problem at hand However as the number of components on a single chip and their performance continue to increase the communication architecture plays a major role in the area performance and energy consumption of the overall system As a result a shift from computation based to communication based design becomes mandatory Towards this end network on chip NoC communication architectures have emerged recently as a promising alternative to classical bus and point to point communication architectures In this dissertation we study outstanding research problems related to modeling analysis and optimization of NoC communication architectures More precisely we present novel design methodologies software tools and FPGA prototypes to aid the design of application specific NoCs

Multi-Core Embedded Systems Georgios Kornaros,2018-10-08 Details a real world product that applies a cutting edge multi core architecture Increasingly demanding modern applications such as those used in telecommunications networking and real time processing of audio video and multimedia streams require multiple processors to achieve computational performance at the rate of a few giga operations per second This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores while being increasingly programmable blending processors and configurable hardware in a power efficient manner Multi Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous processors and heterogeneous multiple cores It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures as well as their limitations and potential for future growth Discusses the available programming models spread across different abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system level parameters It addresses the use of existing open source and free tools originating from several application domains such as traffic modeling graph theory

parallel computing and network simulation In addition the authors cover other important topics associated with multi core embedded systems such as Architectures and interconnects Embedded design methodologies Mapping of applications

Architecture of Computing Systems - ARCS 2011 Mladen Berekovic, William Fornaciari, Uwe Brinkschulte, Cristina Silvano, 2011-02-14 This book constitutes the refereed proceedings of the 24th International Conference on Architecture of Computing Systems ARCS 2011 held in Lake Como Italy in February 2011 The 22 revised full papers presented in seven technical sessions were carefully reviewed and selected from 62 submissions The papers are organized in topical sections on customization and application specific accelerators multi many core architectures adaptive system architectures processor architectures memory architectures optimization organic and autonomic computing network on chip architectures A *Practical Introduction to Hardware/Software Codesign* Patrick R. Schaumont, 2010-09-09 This is a practical book for computer engineers who want to understand or implement hardware software systems It focuses on problems that require one to combine hardware design with software design such problems can be solved with hardware software codesign When used properly hardware software co sign works better than hardware design or software design alone it can improve the overall performance of digital systems and it can shorten their design time Hardware software codesign can help a designer to make trade offs between the exibility and the performance of a digital system To achieve this a designer needs to combine two radically different ways of design the sequential way of dec position in time using software with the parallel way of decomposition in space using hardware Intended Audience This book assumes that you have a basic understanding of hardware that you are miliar with standard digital hardware componentssuch as registers logic gates and components such as multiplexers and arithmetic operators The book also assumes that you know how to write a program in C These topics are usually covered in an introductory course on computer engineering or in a combination of courses on digital design and software engineering **Energy-Efficient Communication Processors** Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies To demonstrate the feasibility of the author s design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes Application Analysis Tools for ASIP Design Kingshuk Karuri, Rainer Leupers, 2011-06-15 This book introduces a novel design methodology which can significantly reduce the ASIP development effort through high degrees of design automation The key elements of this new design methodology are a powerful application profiler and an automated instruction set customization tool which considerably lighten the burden of mapping a target application to an ASIP architecture in the initial design stages The book

includes several design case studies with real life embedded applications to demonstrate how the methodology and the tools can be used in practice for accelerating the overall ASIP design process **System-on-Chip Test Architectures**

Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, 2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students *Managing Temperature Effects in Nanoscale*

Adaptive Systems David Wolpert, Paul Ampadu, 2011-08-31 This book discusses new techniques for detecting controlling and exploiting the impacts of temperature variations on nanoscale circuits and systems A new sensor system is described that can determine the temperature dependence as well as the operating temperature to improve system reliability A new method is presented to control a circuit's temperature dependence by individually tuning pull up and pull down networks to their temperature insensitive operating points This method extends the range of supply voltages that can be made temperature insensitive achieving insensitivity at nominal voltage for the first time On-Chip Networks Natalie Enright, Li-shiuan

Peh, 2022-11-10 With the ability to integrate a large number of cores on a single chip research into on chip networks to facilitate communication becomes increasingly important On chip networks seek to provide a scalable and high bandwidth communication substrate for multi core and many core architectures High bandwidth and low latency within the on chip network must be achieved while fitting within tight area and power budgets In this lecture we examine various fundamental aspects of on chip network design and provide the reader with an overview of the current state of the art research in this field Table of Contents Introduction Interface with System Architecture Topology Routing Flow Control Router

Microarchitecture Conclusions **Network-on-Chip** Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration Network on Chip The Next Generation of System on Chip Integration

examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

VLSI Test Principles and Architectures Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures

Network Processors Ran Giladi, 2008-08-29 Network processors are the basic building blocks of today s high speed high demand quality oriented communication networks Designing and implementing network processors requires a new programming paradigm and an in depth understanding of network processing requirements This book leads the reader through the requirements and the underlying theory of networks network processing and network processors It covers implementation of network processors and integrates EZchip Microcode Development Environment so that you can gain hands on experience in writing high speed networking applications By the

end of the book the reader will be able to write and test applications on a simulated network processor Comprehensive theoretical and practical coverage of networks and high speed networking applications Describes contemporary core metro and access networks and their processing algorithms Covers network processor architectures and programming models enabling readers to assess the optimal network processor type and configuration for their application Free download from <http://www.cse.bgu.ac.il/~npbook/> includes microcode development tools that provide hands on experience with programming a network processor

The Morgan Stanley and d&a European Technology Atlas 2005 , *Autonomic Networking-on-Chip* Phan Cong-Vinh, 2018-09-03 Despite the growing mainstream importance and unique advantages of autonomic networking on chip ANoC technology Autonomic Networking On Chip Bio Inspired Specification Development and Verification is among the first books to evaluate research results on formalizing this emerging NoC paradigm which was inspired by the human nervous system The FIRST Book to Assess Research Results Opportunities Trends in BioChipNets The third book in the Embedded Multi Core Systems series from CRC Press this is an advanced technical guide and reference composed of contributions from prominent researchers in industry and academia around the world A response to the critical need for a global information exchange and dialogue it is written for engineers scientists practitioners and other researchers who have a basic understanding of NoC and are now ready to learn how to specify develop and verify ANoC using rigorous approaches Offers Expert Insights Into Technical Topics Including Bio inspired NoC How to map applications onto ANoC ANoC for FPGAs and structured ASICs Methods to apply formal methods in ANoC development Ways to formalize languages that enable ANoC Methods to validate and verify techniques for ANoC Use of self processes in ANoC self organization configuration healing optimization protection etc Use of calculi for reasoning about context awareness and programming models in ANoC With illustrative figures to simplify contents and enhance understanding this resource contains original peer reviewed chapters reporting on new developments and opportunities emerging trends and open research problems of interest to both the autonomic computing and network on chip communities Coverage includes state of the art ANoC architectures protocols technologies and applications This volume thoroughly explores the theory behind ANoC to illustrate strategies that enable readers to use formal ANoC methods yet still make sound judgments and allow for reasonable justifications in practice

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