Microsystems and Nanosystems

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Micro-Relay Technology for Energy-Efficient Integrated Circuits

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Micro Relay Technology For Energy Efficient Integrated Circuits Microsystems And Nanosystems:

Micro-Relay Technology for Energy-Efficient Integrated Circuits Hei Kam,Fred Chen,2014-10-16 This volume describes the design of relay based circuit systems from device fabrication to circuit micro architectures This book is ideal for both device engineers as well as circuit system designers and highlights the importance of co design across design hierarchies when trying to optimize system performance in this case energy efficiency The book will also appeal to researchers and engineers focused on semiconductor integrated circuits and energy efficient electronics **Design and Demonstration of Integrated Micro-electro-mechanical Relay Circuits for VLSI Applications** Hossein Fariborzi,Massachusetts Institute of Technology. Department of Electrical Engineering and Computer Science,2013 Complementary Metal Oxide Semiconductor CMOS feature size scaling has resulted in significant improvements in the performance and energy efficiency of integrated circuits in the past 4 decades However in the last decade and for technology nodes below 90 nm the scaling of threshold and supply voltages has slowed as a result of subthreshold leakage and power density has increased with each new technology node This has forced a move toward multi core architectures but the energy efficiency benefits of parallelism are limited by the sub thresahold leakage and the minimum energy point for a given function Avoiding this roadblock requires an alternative device with more ideal switching characteristics One promising class of such devices is the electro statically actuated micro electro mechanical MEM relay which offers zero leakage current and abrupt turn on behavior Although a MEM relay is inherently slower than a CMOS transistor due to the mechanical movement we have developed circuit design methodologies to mitigate this problem at the system level This thesis explores such design optimization techniques and investigates the viability of MEM relays as an alternative switching technology for very large scale integration VLSI applications In the first part of this thesis the feasibility of MEM relays for power management applications is discussed Due to their negligibly low leakage in certain applications chips utilizing power gates built with MEM relays can achieve lower total energy than those built with CMOS transistors A simple comparative analysis is presented and provides design guidelines and energy savings estimates as a function of technology parameters and quantifies the further benefits of scaled relay designs We also demonstrate a relay chip successfully power gating a CMOS chip and show a relay based pulse generator suitable for self timed operation Going beyond power gating applications this work also describes circuit techniques and trade offs for logic design with MEM relays focusing on multipliers which are commonly known as the most complex arithmetic units in a digital system These techniques leverage the large disparity between mechanical and electrical time constants of a relay partitioning the logic into large complex gates to minimize the effect of mechanical delay and improve circuit performance At the component design level innovations in compressor unit design minimize the required number of relays for each block and facilitate component cascading with no delay penalty We analyze the area energy delay trade offs vs CMOS designs for typical bit widths and show that scaled relays offer 10 20x lower energy per operation for

moderate throughputs **Advanced Relay Design and Technology for Energy-Efficient Electronics** Jaeseok Jeon,2011 As the era of traditional Complementary Metal Oxide Semiconductor CMOS technology scaling is coming to an end continual improvements in integrated circuit IC performance and cost per function are becoming difficult to achieve without increasing power density This necessitates the investigation of alternate device technologies that surmount the fundamental CMOS energy efficiency limit and hence enable ultra low power ICs To that end a nano electro mechanical NEM relay technology is promising because of its immeasurably low off state leakage current and abrupt turn on behavior which provide for zero static power consumption and potentially very low dynamic power consumption In this dissertation relay design and process technology improvements which led to the successful demonstration of relay based digital IC building blocks are discussed from both device and circuit level perspectives A non volatile NV memory relay design that can enable embedding of NV memory with relay based logic circuits is also discussed In addition multielectrode relays that can lead to smarter design and compact implementation of zero leakage digital integrated circuits are discussed *Nano-Electro-Mechanical (NEM) Relay Devices and Technology for Ultra-Low Energy Digital Integrated Circuits* Rhesa Nathanael,2012 Complementary Metal Oxide Semiconductor CMOS technology scaling has brought about an integrated circuits IC revolution over the past 40 years due to dramatic increases in IC functionality and performance concomitant with reductions in cost per function In the last decade increasing power density has emerged to be the primary barrier to continued rapid advancement in IC technology fundamentally due to non zero transistor off state leakage While innovations in materials transistor structures and circuit system architecture have enabled the semiconductor industry to continue to push the boundaries a fundamental lower limit in energy per operation will eventually be reached A more ideal switching device with zero off state leakage becomes necessary This dissertation proposes a solution to the CMOS power crisis via mechanical computing Specifically robust electro mechanical relay technologies are developed for digital circuit application A 4 Terminal 4T relay design is firstly developed Key technology features include tungsten contacts for high endurance low thermal budget p poly Si0 4Ge0 6 structure for post CMOS process compatibility Al2O3 as a reliable insulation material dry release step to mitigate stiction and folded flexure design to mitigate the impact of residual stress Fabricated relays show good conductance RON IOFF 10 14 A Switching delay in the 100 ns range and endurance exceeding 109 on off cycles is achieved with excellent device yield 95% With relay design and process optimizations pull in voltage below 10 V with less than 1 V hysteresis is achieved Miniaturization reduces the device footprint to 35 mu m 50 mu m 10% of the first generation device footprint 120 mu m 150 mu m Relays with multiple source drain electrodes and multiple gate electrodes are proposed for increased circuit functionality and reduced device count Finally simple relay based logic circuits are demonstrated to show pathways to relay based digital integrated circuits The complementary inverter is the basis for all digital logic circuits and is investigated in depth Relay based logic gates are demonstrated using CMOS like and relay specific design approaches Multi input multi

output relays are proposed to enable any complex logic function to be implemented compactly with only two relays

Nano-electromechanical Relay-based Very-large-scale Integrated Circuits Tian Qin,2017 **Novel Material Integration for Reliable and Energy-Efficient NEM Relay Technology** I-Ru Chen,2014 Energy efficient switching devices have become ever more important with the emergence of ubiquitous computing NEM relays are promising to complement CMOS transistors as circuit building blocks for future ultra low power information processing and as such have recently attracted significant attention from the semiconductor industry and researchers Relay technology potentially can overcome the energy efficiency limit for conventional CMOS technology due to several key characteristics including zero OFF state leakage abrupt switching behavior and potentially very low active energy consumption However two key issues must be addressed for relay technology to reach its full potential surface oxide formation at the contacting surfaces leading to increased ON state resistance after switching and high switching voltages due to strain gradient present within the relay structure This dissertation advances NEM relay technology by investigating solutions to both of these pressing issues Ruthenium whose native oxide is conductive is proposed as the contacting material to improve relay ON state resistance stability Ruthenium contact relays are fabricated after overcoming several process integration challenges and show superior ON state resistance stability in electrical measurements and extended device lifetime The relay structural film is optimized via stress matching among all layers within the structure to provide lower strain gradient below 10E 3 m and hence lower switching voltage These advancements in relay technology along with the integration of a metallic interconnect layer enable complex relay based circuit demonstration In addition to the experimental efforts this dissertation theoretically analyzes the energy efficiency limit of a NEM switch which is generally believed to be limited by the surface adhesion energy New compact **Design Considerations for Nano-Electromechanical Relay Circuits** Matthew Edmund Spencer,2015 Complementary metal oxide semiconductor CMOS technology has a minimum energy per operation and that limitation is one of the myriad hurdles CMOS faces as it reaches small scales This minimum energy is set by the balance between leakage energy and dynamic energy in subthreshold CMOS circuits and sets floors on the achievable energy of digital units A new post CMOS device with a sharper subthreshold slope than CMOS would be able to sidestep this minimum energy constraint A candidate device called a nano electromechancial NEM relay has recently emerged NEM relays are small integrated capacitively actuated mechanical switches The devices have demonstrated extremely high subthreshold slopes ten orders of magnitude over a millivolt of swing However in the same lithographic process they are twenty times larger than a minimum sized CMOS device their gate capacitance is ten times that of a minimum sized CMOS device and their mechanical motion is an order of magnitude slower than a CMOS inverter Can NEM relays improve digital systems even with these drawbacks With proper circuit design simulations say yes This dissertation examines three of the critical components of digital systems logic timing and memory and proposes NEM circuits which mitigate the weaknesses of the technology while achieving design

goals Simulations show that optimized relay logic which arranges for all of the slow movement of relays to happen at the same time can achieve an improvement of 10x in energy per operation below the CMOS minimum energy point at a penalty of 10x in delay and 3x in area This logic style is experimentally demonstrated In addition relay latch based timing with staticization in the feedback path is simulated which results in a working relay pipeline with zero mechanical delays of timing overhead Finally a new device called NEMory is proposed to build dense non volatile mechanical memory A hybrid NEMory CMOS array is simulated and its performance is compared to other memory solutions The NEMory density is higher than any non volatile memory except for multi level cell o chip Flash and its read and write energy are lower than any other non volatile technology Finally the scaling and process limits of realizing mechanical devices are discussed in the context of future work Energy Efficient Circuit Design Using Nanoelectromechanical Relays Ramakrishnan Venkatasubramanian,University of Texas at Dallas. Graduate Program in Electrical Engineering,2012 In nanoscale electromechanical devices dispersion forces like Van der Waals force vdW affect the pull in stability of the relay devices significantly Verilog A electromechanical model of the suspended gate relay operating at 1V with a nominal air gap of 5 10nm has been developed taking into account all the electrical mechanical and dispersion effects

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