



Nanoscale CMOS VLSI Circuits

Design for Manufacturability

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Nanoscale Cmos Vlsi Circuits Design For Manufacturability

Joel Greenberg



Nanoscale Cmos Vlsi Circuits Design For Manufacturability:

Nanoscale CMOS VLSI Circuits: Design for Manufacturability Sandip Kundu, Aswin Sreedhar, 2010-07-08 Cutting Edge CMOS VLSI Design for Manufacturability Techniques This detailed guide offers proven methods for optimizing circuit designs to increase the yield reliability and manufacturability of products and mitigate defects and failure Covering the latest devices technologies and processes Nanoscale CMOS VLSI Circuits Design for Manufacturability focuses on delivering higher performance and lower power consumption Costs constraints and computational efficiencies are also discussed in the practical resource Nanoscale CMOS VLSI Circuits covers Current trends in CMOS VLSI design Semiconductor manufacturing technologies Photolithography Process and device variability analyses and modeling Manufacturing Aware Physical Design Closure Metrology manufacturing defects and defect extraction Defect impact modeling and yield improvement techniques Physical design and reliability DFM tools and methodologies

Nanoscale CMOS VLSI Circuits: Design for Manufacturability Sandip Kundu, Aswin Sreedhar, 2010-06-22 Cutting Edge CMOS VLSI Design for Manufacturability Techniques This detailed guide offers proven methods for optimizing circuit designs to increase the yield reliability and manufacturability of products and mitigate defects and failure Covering the latest devices technologies and processes Nanoscale CMOS VLSI Circuits Design for Manufacturability focuses on delivering higher performance and lower power consumption Costs constraints and computational efficiencies are also discussed in the practical resource Nanoscale CMOS VLSI Circuits covers Current trends in CMOS VLSI design Semiconductor manufacturing technologies Photolithography Process and device variability analyses and modeling Manufacturing Aware Physical Design Closure Metrology manufacturing defects and defect extraction Defect impact modeling and yield improvement techniques Physical design and reliability DFM tools and methodologies

Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide Trent McConaghy, Kristopher Breen, Jeffrey Dyck, Amit Gupta, 2012-10-02 This book targets custom IC designers who are encountering variation issues in their designs especially for modern process nodes at 45nm and below such as statistical process variations environmental variations and layout effects It teaches them the state of the art in Variation Aware Design tools which help the designer to analyze quickly the variation effects identify the problems and fix the problems Furthermore this book describes the algorithms and algorithm behavior performance limitations which is of use to designers considering these tools designers using these tools CAD researchers and CAD managers

Analysis and Design of Resilient VLSI Circuits Rajesh Garg, 2009-10-22 This monograph is motivated by the challenges faced in designing reliable VLSI systems in modern VLSI processes The reliable operation of integrated circuits ICs has become increasingly difficult to achieve in the deep submicron DSM era With continuously decreasing device feature sizes combined with lower supply voltages and higher operating frequencies the noise immunity of VLSI circuits is decreasing alarmingly Thus VLSI circuits are becoming more vulnerable to noise effects such as crosstalk power supply variations and radiation induced soft errors

Among these noise sources soft errors or error caused by radiation particle strikes have become an increasingly troublesome issue for memory arrays as well as combinational logic circuits. Also in the DSM era process variations are increasing at a significant rate making it more difficult to design reliable VLSI circuits. Hence it is important to efficiently design robust VLSI circuits that are resilient to radiation particle strikes and process variations. The work presented in this research monograph presents several analysis and design techniques with the goal of realizing VLSI circuits which are radiation and process variation tolerant.

Reliability of Nanoscale Circuits and Systems Miloš Stanisavljević, Alexandre Schmid, Yusuf Leblebici, 2010-10-20 This book is intended to give a general overview of reliability faults, fault models, nanotechnology nanodevices, fault tolerant architectures and reliability evaluation techniques. Additionally, the book provides an in-depth state of the art, research results and methods for fault tolerance as well as the methodology for designing fault tolerant systems out of highly unreliable components.

Embedded Memories for Nano-Scale VLSIs Kevin Zhang, 2009-04-21 Kevin Zhang Advancement of semiconductor technology has driven the rapid growth of very large scale integrated VLSI systems for increasingly broad applications including high end and mobile computing, consumer electronics such as 3D gaming, multi-function or smart phone and various set top players and ubiquitous sensor and medical devices. To meet the increasing demand for higher performance and lower power consumption in many different system applications, it is often required to have a large amount of on-die or embedded memory to support the need of data bandwidth in a system. The varieties of embedded memory in a given system have also become increasingly more complex, ranging from static to dynamic and volatile to nonvolatile. Among embedded memories, six-transistor 6T-based static random access memory (SRAM) continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology. But as the technology scaling continues, SRAM design is facing severe challenge in maintaining sufficient cell stability margin under relentless area scaling. Meanwhile, rapid expansion in mobile application, including new emerging application in sensor and medical devices, requires far more aggressive voltage scaling to meet very stringent power constraint. Many innovative circuit topologies and techniques have been extensively explored in recent years to address these challenges.

Dependable Multicore Architectures at Nanoscale Marco Ottavi, Dimitris Gizopoulos, Salvatore Pontarelli, 2017-08-28 This book provides comprehensive coverage of the dependability challenges in today's advanced computing systems. It is an in-depth discussion of all the technological and design level techniques that may be used to overcome these issues and analyzes various dependability assessment methods. The impact of individual application scenarios on the definition of challenges and solutions is considered so that the designer can clearly assess the problems and adjust the solution based on the specifications in question. The book is composed of three sections beginning with an introduction to current dependability challenges arising in complex computing systems implemented with nanoscale technologies and of the effect of the application scenario. The second section details all the fault tolerance techniques that are applicable in the manufacture of

reliable advanced computing devices Different levels from technology level fault avoidance to the use of error correcting codes and system level checkpointing are introduced and explained as applicable to the different application scenario requirements Finally the third section proposes a roadmap of future trends in and perspectives on the dependability and manufacturability of advanced computing systems from the special point of view of industrial stakeholders Dependable Multicore Architectures at Nanoscale showcases the original ideas and concepts introduced into the field of nanoscale manufacturing and systems reliability over nearly four years of work within COST Action IC1103 MEDIAN a think tank with participants from 27 countries Academic researchers and graduate students working in multi core computer systems and their manufacture will find this book of interest as will industrial design and manufacturing engineers working in VLSI companies

Design for Manufacturability and Yield for Nano-Scale CMOS Charles Chiang,Jamil Kawa,2007-06-15 This book walks the reader through all the aspects of manufacturability and yield in a nano CMOS process It covers all CAD CAE aspects of a SOC design flow and addresses a new topic DFM DFY critical at 90 nm and beyond This book is a must read book the serious practicing IC designer and an excellent primer for any graduate student intent on having a career in IC design or in EDA tool development

Nano-CMOS Design for Manufacturability Ban P. Wong,Anurag Mittal,Greg W. Starr,Franz Zach,Victor Moroz,Andrew Kahng,2008-12-29 Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano CMOS Design for Manufacturability examines the challenges that design engineers face in the nano scaled era such as exacerbated effects and the proven design for manufacturability DFM methodology in the midst of increasing variability and design process interactions In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore s law the authors also tackle complex issues in the design process to overcome the difficulties including the use of a functional first silicon to support a predictable product ramp Moreover they introduce several emerging concepts including stress proximity effects contour based extraction and design process interactions This book is the sequel to Nano CMOS Circuit and Physical Design taking design to technology nodes beyond 65nm geometries It is divided into three parts Part One Newly Exacerbated Effects introduces the newly exacerbated effects that require designers attention beginning with a discussion of the lithography aspects of DFM followed by the impact of layout on transistor performance Part Two Design Solutions examines how to mitigate the impact of process effects discussing the methodology needed to make sub wavelength patterning technology work in manufacturing as well as design solutions to deal with signal power integrity WELL stress proximity effects and process variability Part Three The Road to DFM describes new tools needed to support DFM efforts including an auto correction tool capable of fixing the layout of cells with multiple optimization goals followed by a look ahead into the future of DFM Throughout the book real world examples simplify complex concepts helping readers see how they can successfully handle projects on Nano CMOS nodes It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and in short

make designs that are not only functional but that also meet power and performance goals within the design schedule

Design for Manufacturability and Statistical Design Michael Orshansky, Sani Nassif, Duane Boning, 2007-10-28 Design for Manufacturability and Statistical Design A Constructive Approach provides a thorough treatment of the causes of variability methods for statistical data characterization and techniques for modeling analysis and optimization of integrated circuits to improve yield The objective of the constructive approach developed in this book is to formulate a consistent set of methods and principles necessary for rigorous statistical design and design for manufacturability from device physics to large scale circuit optimization The segments of the book are devoted respectively to understanding the causes of variability design of test structures for variability characterization statistically rigorous data analysis techniques of design for manufacturability in lithography and in chemical mechanical polishing statistical simulation analysis and optimization techniques for improving parametric yield Design for Manufacturability and Statistical Design A Constructive Approach presents an overview of the methods that need to be mastered for state of the art design for manufacturability and statistical design methodologies It is an important reference for practitioners and students in the field of computer aided design of integrated circuits

Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray

sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes

Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation Rene van Leuken, Gilles Sicard, 2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed circuits process variation high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic

Lifetime Reliability-aware Design of Integrated Circuits Mohsen Raji, Behnam Ghavami, 2022-11-16 This book covers the state of the art research in design of modern electronic systems used in safety critical applications such as medical devices aircraft flight control and automotive systems The authors discuss lifetime reliability of digital systems as well as an overview of the latest research in the field of reliability aware design of integrated circuits They address modeling approaches and techniques for evaluation and improvement of lifetime reliability for nano scale CMOS digital circuits as well as design algorithms that are the cornerstone of Computer Aided Design CAD of reliable VLSI circuits In addition to developing lifetime reliability analysis and techniques for clocked storage elements such as flip flops the authors also describe analysis and improvement strategies targeting commercial digital circuits

Low Power Circuits for Emerging Applications in Communications, Computing, and Sensing Fei Yuan, 2018-12-07 The book addresses the need to investigate new approaches to lower energy requirement in multiple application areas and serves as a guide into emerging circuit technologies It explores revolutionary device concepts sensors and associated circuits and architectures that will greatly extend the practical engineering limits of energy efficient computation The book responds to the need to develop disruptive new system architectures circuit microarchitectures and attendant device and interconnect technology aimed at achieving the highest level of computational energy efficiency for general purpose computing systems Features Discusses unique technologies and material only available in specialized journal and conferences Covers emerging applications areas such as ultra low power communications emerging bio electronics and operation in extreme environments Explores broad circuit operation ex analog RF memory and digital circuits Contains practical applications in the engineering field as well as graduate studies Written by international experts from both academia and industry

Diagnostic Devices with Microfluidics Francesco Piraino, Šeila Selimović, 2017-06-26 This book provides a current view of the research and commercial landscape of diagnostics devices particularly those that utilize microscale technologies intended for both patient and laboratory use Common diagnostic devices that are based on microfluidic principles include glucose sensors for diabetic patients and over the counter pregnancy tests Other diagnostic devices are being developed to quickly test a patient for bacterial and viral infections and

other diseases The chapters written by experts from around the world discuss how to fabricate apply and market microfluidic diagnostic chips for lab and at home use Most importantly the book also contains a discussion of topics relevant to the private sector including patient focused market oriented development of diagnostics devices Chapter 9 of this book is freely available as a downloadable Open Access PDF under a CC BY 3 0 license https://s3-us-west-2.amazonaws.com/tandfbis-rt-files/docs/OpenAccessChapters/9781498772938_oachapter9.pdf *Circuits at the Nanoscale* Krzysztof Iniewski, 2018-10-08

Circuits for Emerging Technologies Beyond CMOS New exciting opportunities are abounding in the field of body area networks wireless communications data networking and optical imaging In response to these developments top notch international experts in industry and academia present *Circuits at the Nanoscale Communications Imaging and Sensing* This volume unique in both its scope and its focus addresses the state of the art in integrated circuit design in the context of emerging systems A must for anyone serious about circuit design for future technologies this book discusses emerging materials that can take system performance beyond standard CMOS These include Silicon on Insulator SOI Silicon Germanium SiGe and Indium Phosphide InP Three dimensional CMOS integration and co integration with Microelectromechanical MEMS technology and radiation sensors are described as well Topics in the book are divided into comprehensive sections on emerging design techniques mixed signal CMOS circuits circuits for communications and circuits for imaging and sensing Dr Krzysztof Iniewski is a director at CMOS Emerging Technologies Inc a consulting company in Vancouver British Columbia His current research interests are in VLSI circuits for medical applications He has published over 100 research papers in international journals and conferences and he holds 18 international patents granted in the United States Canada France Germany and Japan In this volume he has assembled the contributions of over 60 world renowned experts who are at the top of their field in the world of circuit design advancing the bank of knowledge for all who work in this exciting and burgeoning area

Semiconductor Devices in Harsh Conditions Kirsten Weide-Zaage, Malgorzata Chrzanowska-Jeske, 2016-11-25 This book introduces the reader to a number of challenges for the operation of electronic devices in various harsh environmental conditions While some chapters focus on measuring and understanding the effects of these environments on electronic components many also propose design solutions whether in choice of material innovative structures or strategies for amelioration and repair Many applications need electronics designed to operate in harsh environments Readers will find in this collection of topics tools and ideas useful in their own pursuits and of interest to their intellectual curiosity With a focus on radiation operating conditions sensor systems package and system design the book is divided into three parts The first part deals with sensing devices designed for operating in the presence of radiation commercial off the shelf COTS products for space computing and influences of single event upset The second covers system and package design for harsh operating conditions The third presents devices for biomedical applications under moisture and temperature loads in the frame of sensor systems and operating conditions *Nanoscale Memory Repair* Masashi

Horiguchi,Kiyoo Itoh,2011-01-11 Yield and reliability of memories have degraded with device and voltage scaling in the nano scale era due to ever increasing hard soft errors and device parameter variations This book systematically describes these yield and reliability issues in terms of mathematics and engineering as well as an array of repair techniques based on the authors long careers in developing memories and low voltage CMOS circuits Nanoscale Memory Repair gives a detailed explanation of the various yield models and calculations as well as various practical logic and circuits that are critical for higher yield and reliability

X-Ray Diffraction Imaging Joel Greenberg,2018-11-02 This book explores novel methods for implementing X ray diffraction technology as an imaging modality which have been made possible through recent breakthroughs in detector technology computational power and data processing algorithms The ability to perform fast spatially resolved X ray diffraction throughout the volume of a sample opens up entirely new possibilities in areas such as material analysis cancer diagnosis and explosive detection thus offering the potential to revolutionize the fields of medical security and industrial imaging and detection Featuring chapters written by an international selection of authors from both academia and industry the book provides a comprehensive discussion of the underlying physics architectures and applications of X ray diffraction imaging that is accessible and relevant to neophytes and experts alike Teaches novel methods for X ray diffraction imaging Comprehensive and self contained discussion of the relevant physics imaging techniques system components and data processing algorithms Features state of the art work of international authors from both academia and industry Includes practical applications in the medical industrial and security sectors

Energy Efficient Computing & Electronics Santosh K. Kurinec,Sumeet Walia,2019-01-31 In our abundant computing infrastructure performance improvements across most all application spaces are now severely limited by the energy dissipation involved in processing storing and moving data The exponential increase in the volume of data to be handled by our computational infrastructure is driven in large part by unstructured data from countless sources This book explores revolutionary device concepts associated circuits and architectures that will greatly extend the practical engineering limits of energy efficient computation from device to circuit to system level With chapters written by international experts in their corresponding field the text investigates new approaches to lower energy requirements in computing Features Has a comprehensive coverage of various technologies Written by international experts in their corresponding field Covers revolutionary concepts at the device circuit and system levels

Whispering the Strategies of Language: An Psychological Journey through **Nanoscale Cmos Vlsi Circuits Design For Manufacturability**

In a digitally-driven earth where monitors reign supreme and immediate communication drowns out the subtleties of language, the profound strategies and emotional nuances hidden within phrases often get unheard. Yet, set within the pages of **Nanoscale Cmos Vlsi Circuits Design For Manufacturability** a interesting literary treasure pulsing with fresh thoughts, lies a fantastic journey waiting to be undertaken. Published by an experienced wordsmith, this wonderful opus attracts readers on an introspective trip, softly unraveling the veiled truths and profound affect resonating within the very cloth of each word. Within the mental depths of this poignant review, we can embark upon a genuine exploration of the book is key styles, dissect its interesting publishing fashion, and yield to the effective resonance it evokes deep within the recesses of readers hearts.

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