Bei Yu · David Z. Pan

Design for Manufacturability with Advanced Lithography

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Design for Manufacturability with Advanced Lithography Bei Yu,David Z. Pan,2015-10-28 This book introduces readers to the most advanced research results on Design for Manufacturability DFM with multiple patterning lithography MPL and electron beam lithography EBL The authors describe in detail a set of algorithms methodologies to resolve issues in modern design for manufacturability problems with advanced lithography Unlike books that discuss DFM from the product level or physical manufacturing level this book describes DFM solutions from a circuit design level such that most of the critical problems can be formulated and solved through combinatorial algorithms *Who's Who in Science and Engineering 2008-2009* Who's Who Marquis,Marquis Who's Who,2007-12 **Who's who in Finance and Business** ,2004 *American Manufacturers Directory* ,1998 *Government Reports Announcements & Index* ,1993-02 **Lithography-driven Design for Manufacturing in Nanometer-era VLSI** Chul-Hong Park,2008 Photolithography has been a key enabler of the aggressive IC technology scaling implicit in Moore s Law As minimum feature sizes approach the physical limits of lithography and the manufacturing process resolution enhancement techniques RETs dictate certain tradeoffs with various aspects of process and performance This in turn has led to unpredictable design unpredictable manufacturing and low yield As a result close communication between designer and manufacturer has become essential to overcome the uncertainties of design and manufacturing The design for manufacturability DFM paradigm has emerged recently to improve communications at the design manufacturing interface and to reduce manufacturing variability DFM is a set of technologies and methodologies that both help the designer extract maximum value from silicon process technology and solve unsolvable manufacturing challenges Traditional DFM techniques which include design rule check DRC and optical proximity correction OPC have been successfully used until now However as the extent and complexity of lithography variations increase traditional techniques are no longer adequate to accommodate the various lithography demands This thesis focuses on ways to mitigate the impact of lithography variations on design by establishing new interfaces between design and manufacturing The motivations for doing so are improved printability timing and leakage as well as reduced design cost To improve printability we propose a detailed placement perturbation technique for improved depth of focus and process window Using a dynamic programming DP based method for the perturbation the technique facilitates insertion of scattering bars and etch dummy features reducing inter cell forbidden pitches almost completely We also propose a novel auxiliary pattern enabled cell based OPC which can improve the edge placement error over cell based OPC The technique improves runtime which has grown unacceptably in model based OPC while retaining its runtime advantage as well as timing and leakage optimization The detailed placement framework is also available to allow opportunistic insertion of auxiliary pattern around cell instances in the design layout Aberration leads to linewidth variation which is fundamental to achieve timing performance and manufacturing yield We describe an aberration aware timing analysis flow that accounts for aberration induced cell delay variations We then propose an aberration aware timing driven global placement technique which utilizes the predictable slow and fast regions created on the chip due to aberration to improve cycle time The use of the technique along with field blading achieves significant cycle time improvement DoseMapper technique adopted in advanced lithography equipments has been used to reduce the across chip linewidth variation We propose a novel method to enhance timing yield as well as reduce leakage power by combined dose map and placement optimizations The new dose map is not determined to have the same critical dimension CD in all transistor gates but optimized to have different linewidths That is for devices on setup timing critical paths a smaller than nominal CD will be desirable since this creates a faster switching transistor On the other hand for devices on hold timing critical paths a larger than nominal gate CD will be desirable since this creates a less leaky transistor Last the golden verification signoff tool using simulation based approach represents a runtime quality tradeoff that is high in quality but also high in runtime We are motivated to develop a low runtime pre filter that reduces the amount of layout area to be analyzed by the golden tool without compromising the overall quality finding hotspots We demonstrate a dual graph based hotspot filtering technique that enables fast and accurate estimation **Physical Design and Mask Synthesis for Directed Self-Assembly Lithography** Seongbo Shim,Youngsoo Shin,2018-03-21 This book discusses physical design and mask synthesis of directed self assembly lithography DSAL It covers the basic background of DSAL technology physical design optimizations such as placement and redundant via insertion and DSAL mask synthesis as well as its verification Directed self assembly lithography DSAL is a highly promising patterning solution in sub 7nm technology

Lithography Aware Physical Design and Layout Optimization for Manufacturability Jhih-Rong Gao,2014 As technology continues to scale down semiconductor manufacturing with 193nm lithography is greatly challenging because the required half pitch size is beyond the resolution limit In order to bridge the gap between design requirements and manufacturing limitations various resolution enhancement techniques have been proposed to avoid potentially problematic patterns and to improve product yield In addition co optimization between design performance and manufacturability can further provide flexible and significant yield improvement and it has become necessary for advanced technology nodes This dissertation presents the methodologies to consider the lithography impact in different design stages to improve layout manufacturability Double Patterning Lithography DPL has been a promising solution for sub 22nm node volume production Among DPL techniques self aligned double patterning SADP provides good overlay controllability when two masks are not aligned perfectly However SADP process places several limitations on design flexibility and still exists many challenges in physical design stages Starting from the early design stage we analyze the standard cell designs and construct a set of SADP aware cell placement candidates and show that placement legalization based on this SADP awareness information can effectively resolve DPL conflicts In the detailed routing stage we propose a new routing cost formulation based on SADP compliant routing guidelines and achieve routing and layout decomposition simultaneously In the case that limited routing perturbation is allowed we propose a post routing flow based on lithography simulation and lithography aware design rules Both routing methods one in detailed routing stage and one in post routing stage reduce DPL conflicts violations significantly with negligible wire length impact In the layout decomposition stage layout modification is restricted and thus the manufacturability is even harder to guaranteed By taking the advantage of complementary lithography we present a new layout decomposition approach with e beam cutting which optimizes SADP overlay error and e beam lithography throughput simultaneously After the mask layout is defined optical proximity correction OPC is one of the resolution enhancement techniques that is commonly required to compensate the image distortion from the lithography process We propose an inverse lithography technique to solve the OPC problem considering design target and process window co optimization Our mask optimization is pixel based and thus can enable better contour fidelity In the final physical verification stage a complex and time consuming lithography simulation needs to be performed to identify faulty patterns We provide a classification method based on support vector machine and principle component analysis that detects lithographic hotspots efficiently and accurately **Design Automation Algorithms for Advanced Lithography** Zigang Xiao,2015 **Optimization for Advanced Lithography** ,2014 *Design for Manufacturing with Directed Self-assembly Lithography* Jiaojiao Ou,2018 In ultra scaled very large scale integration VLSI lithography has become the bottleneck in integrated circuit IC fabrication Since the conventional 193nm immersion lithography has reached the resolution limit multiple patterning MP is adopted in order to meet the pitch requirement of ultra scaled design However the manufacturing cost also increases dramatically with the growth of number of masks at the same time Therefore industries are looking for alternative lithography techniques to extend the 193nm immersion lithography to the sub 7nm nodes With the continuous delaying of Extreme Ultraviolet EUV Directed Self Assembly DSA lithography has emerged as one of the promising alternative lithography techniques due to its low cost high throughput and its ability to multiply the pitch of lines and vias DSA has been intensively explored by both industry and academia in recent years Memory and the dense via layer in logic might be the first application of DSA lithography in the mainstream IC production DSA can also be applied on fabrication of cut masks to reduce the overall wire extensions However there are still many challenges such as defectivity line edge roughness and placement accuracy which prevent DSA from the high volume manufacturing Integrating this technology into the fab flow and designing circuit around it also remain to be problematic Considering the limitations and constraints of the topologies of DSA this dissertation investigates and proposes novel algorithms for the DSA aware design problem in the areas of design for manufacturability and physical design First a DSA based cut mask optimization for unidirectional design is proposed Efficient algorithm is developed to assign DSA guiding template to metal line ends to minimize wire extensions and conflicts Second as redundant via insertion has been widely used in the post routing stage to improve the yield but the insertion of more vias introduces challenges for DSA patterning This dissertation proposes a novel approach to perform the DSA aware redundant via insertion to improve the redundant via insertion rate and DSA compatibility Since both via grouping and DSA guiding template decomposition are the essential problems for DSA aware design which should be solved concurrently this dissertation also proposes an efficient algorithm to solve this problem Considering multiple patterning has already been used in DSA lithography a coherent work including single block copolymer BCP and double block copolymer guiding template assignment is proposed for DSA and multiple pattering hybrid lithography In addition it is also noticed that optimization in the post routing stage is not enough to eliminate DSA patterning violations thus this dissertation also proposes the DSA compliant detailed routing algorithm with concurrent double pattering and guiding templates assignment **Design for Manufacturability and Reliability Through Learning and Optimization** Wei Ye (Ph. D.),2020 Modern society relies on technologies with integrated circuits ICs at their heart In the last several decades as the performance and complexity of ICs keep escalating the semiconductor industry has demonstrated an ability to develop new process techniques and product designs that are both manufacturable and reliable However as the transistor feature size is further shrunk into extreme scaling e g 10 nm and beyond large scale integration of transistors and interconnects brings ever increasing challenges revolving around manufacturability and reliability The major issues in manufacturability and reliability for modern ICs come from three aspects 1 layout dependent manufacturability e g manufacturing yield sensitive to design patterns 2 time consuming process modeling e g complex lithography systems 3 design sensitive reliability e g lifetime related to layout designs In order to close the gap between design and manufacturing and enhance design reliability automated layout generation requires cross layer information feed forward and feedback such as accurate process modeling and reliability guided design optimization This dissertation attempts to address the aforementioned challenges in manufacturing closure and reliability signoff through efficient machine learning techniques for lithography hotspot detection and lithography modeling and synergistic design optimization for electromigration EM Our research includes efficient lithography hotspot detection learning based lithography modeling and EM aware physical design to achieve efficient manufacturing closure and reliability signoff For lithography hotspot detection due to the increasingly complicated design patterns early and quick feedback for lithography hotspots is desired to guide design closure in early stages Machine learning approaches have been successfully applied to hotspot detection while demonstrating a remarkable capability of generalization to unseen hotspot patterns However most of the proposed machine learning approaches are not yet able to answer two critical questions model confidence and model efficiency This study develops a lithography hotspot detection framework capable of providing modeling confidence with fewer training data and fewer expensive lithography simulations needed and also provides a holistic measure for the intrinsic class imbalance in lithography hotspot detection For lithography modeling one of the major limitations in process modeling is considered the trade off between modeling efficiency and accuracy The steady decrease of the feature sizes along with the growing complexity and variation of the manufacturing process has tremendously increased the lithography modeling complexity and prolonged the already slow simulation procedure Different modeling frameworks are proposed in this study leveraging recent advancements in machine learning particularly generative adversarial learning to generate virtually simulated silicon image efficiently without running detailed optical simulations With our proposed deep learning techniques a significant improvement in modeling efficiency is achieved while maintaining high modeling accuracy For EM aware physical design we demonstrate the limitation of conventional design and EM signoff flow when faced with the ever growing EM violations in advanced technology nodes Two essential directions are explored with practical algorithms and new design flows 1 Power grid EM detection and optimization with several detailed placement techniques 2 Learning based signal EM prediction and mitigation at different physical design stages The effectiveness of proposed design optimization and machine learning techniques is demonstrated with extensive experiments on industrial strength benchmarks Our approaches are capable of reducing turn around time saving modeling costs and enabling fast manufacturing closure and reliability signoff *Lithography for Semiconductor Manufacturing* ,1999 **Computer Based Design and Manufacturing** Emad Abouel Nasr,Ali K. Kamrani,2010-10-29 This book offers insights into the methods and techniques required to implement a consumer focused product design philosophy It does this by integrating capabilities for intelligent information support and group decision making utilizing a common enterprise network model and knowledge interface through shared technologies It includes discussion of applied methods developed in the field of the product design and gives the latest research results *Design-Process-Technology Co-optimization for Manufacturability XIII* Jason P. Cain,2019

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